

# 042N100TA / 042N100TB

## 100V N-Channel Super Trench Power MOSFET



### Description

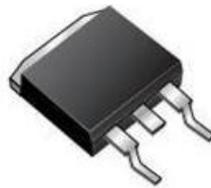
042N100T uses Super Trench technology that is uniquely optimized to provide the most efficient high frequency switching performance. Both conduction and switching power losses are minimized due to an extremely low combination of  $R_{DS(ON)}$  and  $Q_g$ . This device is ideal for high-frequency switching and synchronous rectification.

### General Features

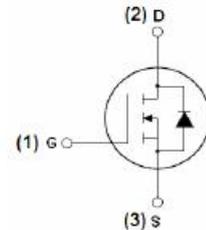
- Excellent gate charge x  $R_{DS(on)}$  product(FOM)
- Very low on-resistance  $R_{DS(on)}$
- Pb-free lead plating



042N100TA



042N100TB



### MAIN CHARACTERISTICS

<b>ID</b>	<b>110A</b>
<b>VDSS</b>	<b>100v</b>
<b><math>R_{DS(ON)Typ}</math> (at VGS=10V) TO-220</b>	<b>3.7mΩ</b>
<b><math>R_{DS(ON)Typ}</math> (at VGS=10V) TO-263</b>	<b>3.6mΩ</b>

### Application

- DC/DC Converter
- Ideal for high-frequency
- Switching and synchronousrectification

### Absolute maximum ratings

Symbol	Parameter	042N100TA	042N100TB	Unit
$V_{DSS}$	Drain-source voltage	100		V
$V_{GSS}$	Gate-Source Voltage	$\pm 20$		V
$I_D$	Drain Current -continuous( $T_C=25^\circ C$ )	110		A
	Drain Current -continuous( $T_C=100^\circ C$ )	95		
$I_{DM}$	Drain Current-Pulsed	520		A
$P_D$	Power Dissipation	$T_c=25^\circ C$	220	W
		Derating factor	1.43	W/ $^\circ C$
$E_{AS}$	Single pulsed avalanche energy (Note5)	750		mJ

### Thermal Characteristics

Symbol	Parameter	042N100TA	042N100TB	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note2)	0.67		$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	52		$^\circ C/W$

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Electrical Characteristics  $T_C=25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Conditions	Min.	Typ.	Max	Unit
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain Source breakdown voltage	$V_{GS}=0V, I_D=250\mu A, T_J=25^\circ\text{C}$	100	-	-	V
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 200$	nA

**On Characteristics (Note 3)**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	2		4	V	
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS}=10V, I_D=50A$	TO-220	-	3.7	4.2	$m\Omega$
			TO-263	-	3.6	4.2	$m\Omega$
$G_{FS}$	Forward Transconductance	$V_{DS}=5V, I_D=50A$	-	90	-	S	

**Dynamic Characteristics (Note 4)**

$C_{iss}$	Input Capacitance	$V_{DS}=50V, V_{GS}=0V, F=1\text{MHz}$	-	6998	-	pF
$C_{oss}$	Output Capacitance		-	892	-	pF
$C_{rss}$	Reverse Transfer Capacitance		-	32	-	pF

**SWITCHING Characteristics (Note 4)**

$T_{D(on)}$	Turn-on Delay Time	$V_{DD}=50V, I_D=50A, R_G=1.6\Omega, V_{GS}=10V$	-	22	-	ns
$T_r$	Turn-on Rise Time		-	11.8	-	ns
$T_{D(off)}$	Turn-off Delay Time		-	46	-	ns
$T_f$	Turn-off Fall Time		-	10.5	-	ns
$Q_g$	Total Gate Charge	$V_{DS}=50V, I_D=100A, V_{GS}=10V$	-	106	-	nC
$Q_{gs}$	Gate Source Charge		-	36	-	nC
$Q_{gd}$	Gate Drain Charge		-	25	-	nC

**Drain-Source Diode Characteristics and Maximum Ratings**

$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS}=0V, I_S=50A$	-	-	1.2	V
$T_{rr}$	Reverse Recovery Time	$T_J=25^\circ\text{C}, V_R=50V, I_F=30A, di/dt=100A/\mu S$ (Note3)	-	155	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	390	-	$\mu C$

### Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse test: Pulse Width  $\leq 300\mu S$ , Duty Cycle  $\leq 2\%$
4. Guaranteed by design, not subject to production
5. EAS condition:  $T_J=25^\circ\text{C}, V_{DD}=50V, V_G=10V, L=0.5\text{mH}, R_g=25\Omega$



TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS (Curves)

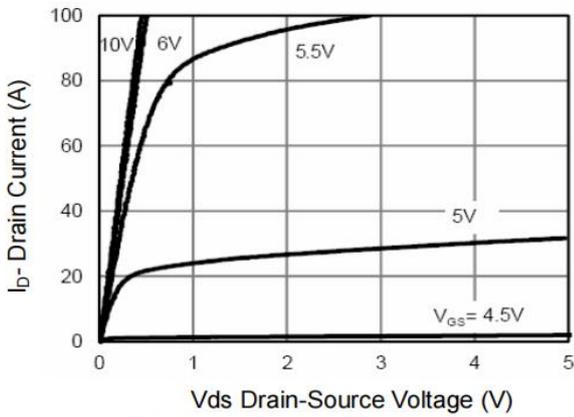


Figure 1 Output Characteristics

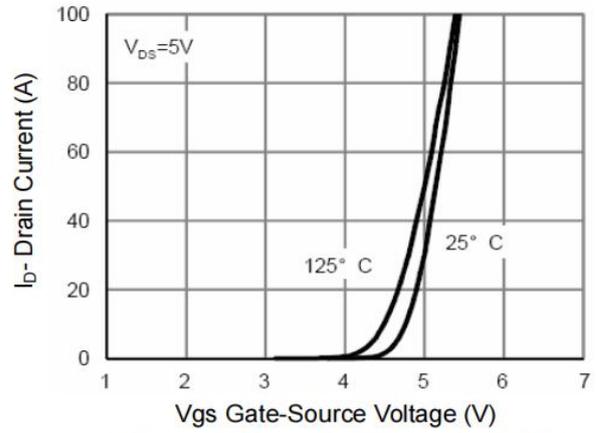


Figure 2 Transfer Characteristics

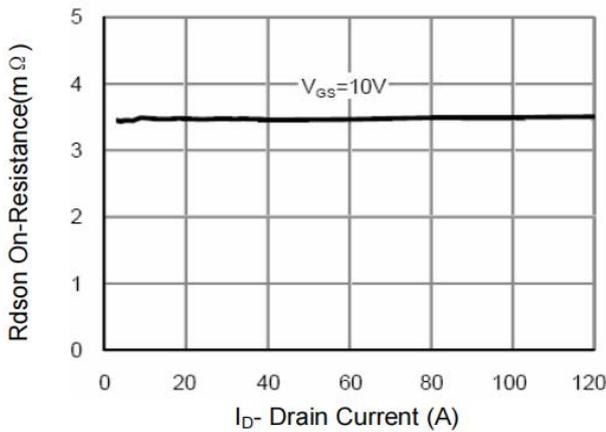


Figure 3 Rdson- Drain Current

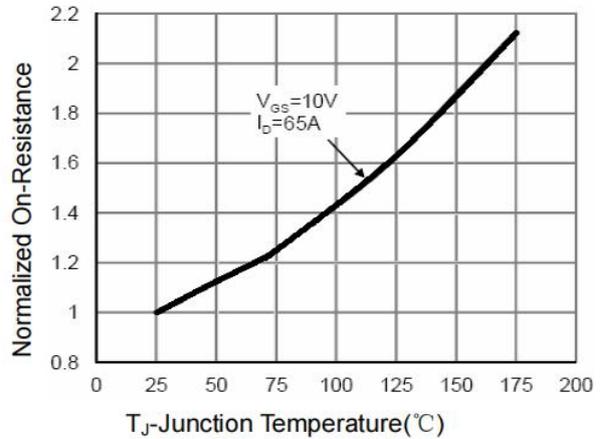


Figure 4 Rdson-Junction Temperature

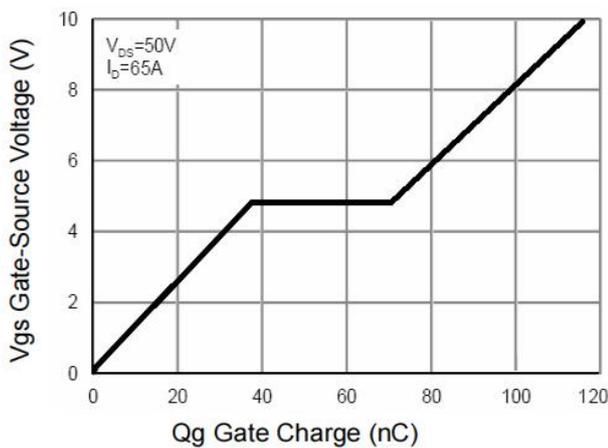


Figure 5 Gate Charge

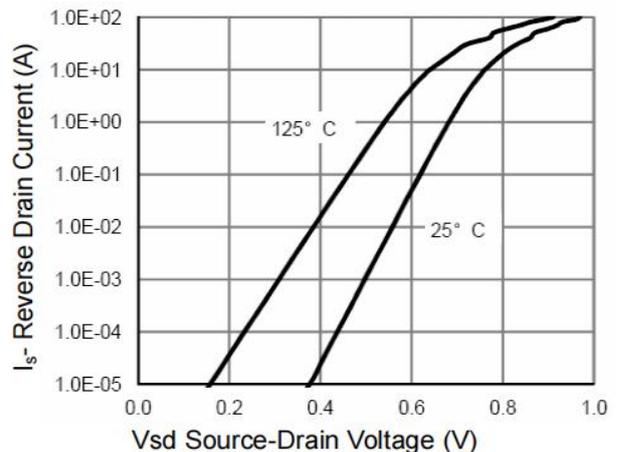
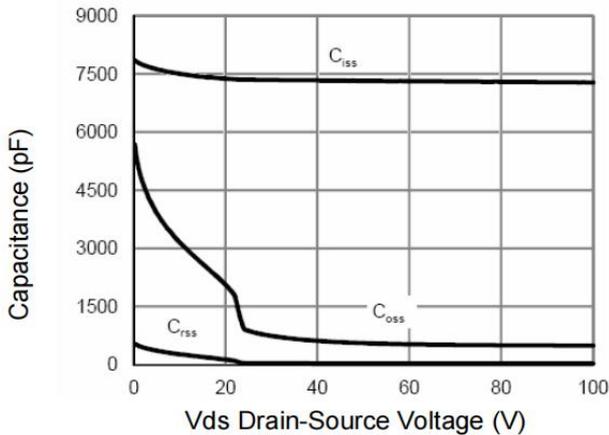


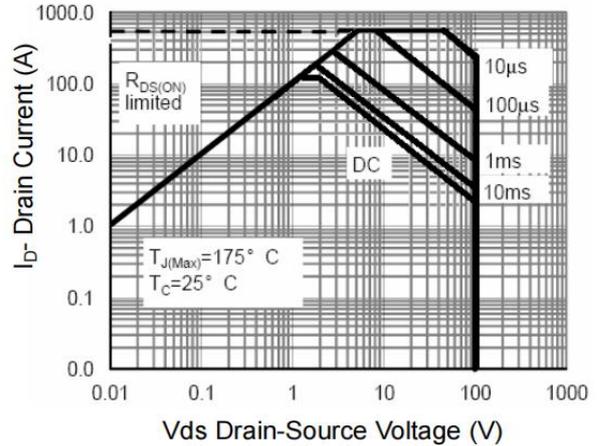
Figure 6 Source- Drain Diode Forward

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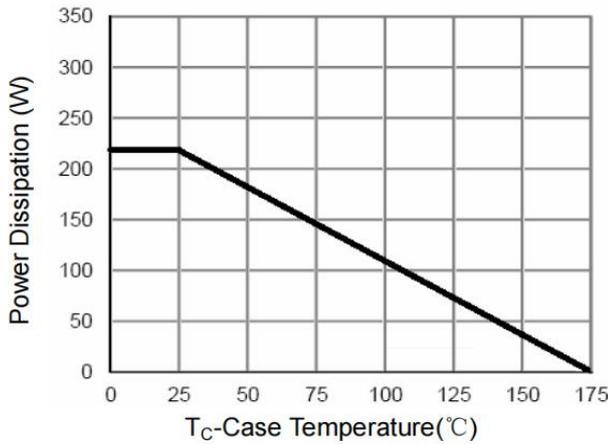
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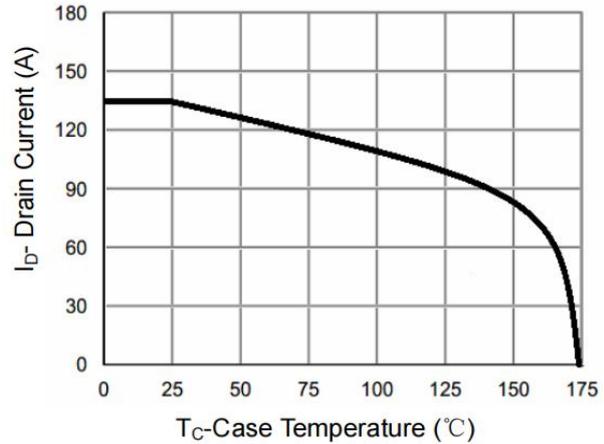
**Figure 7 Capacitance vs Vds**



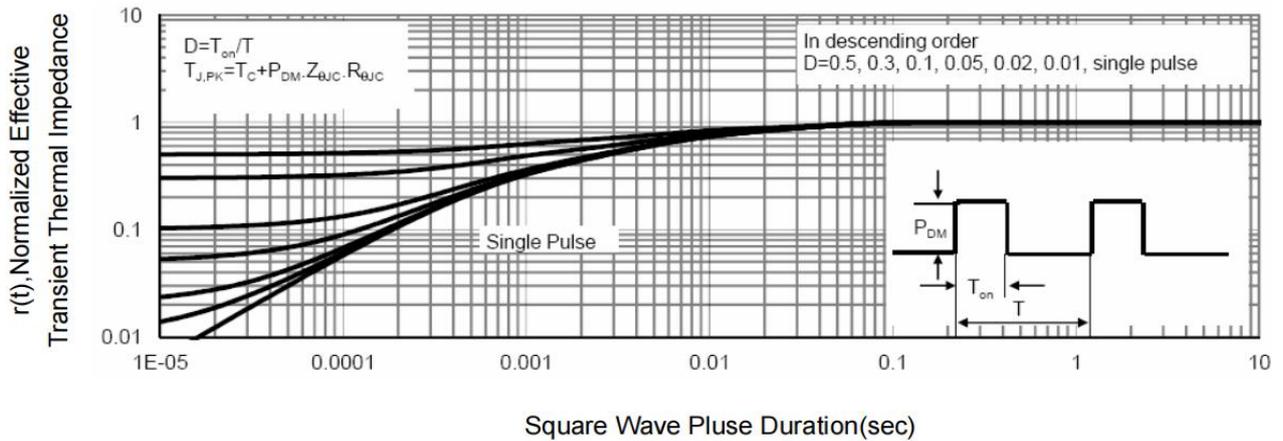
**Figure 8 Safe Operation Area**



**Figure 9 Power De-rating**



**Figure 10 Current De-rating**



**Figure 11 Normalized Maximum Transient Thermal Impedance**

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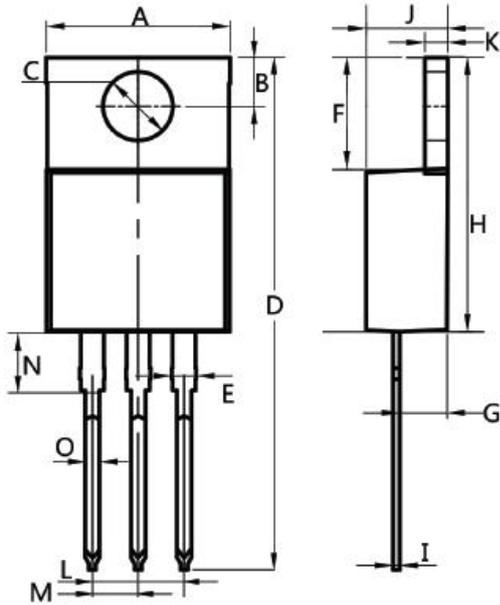
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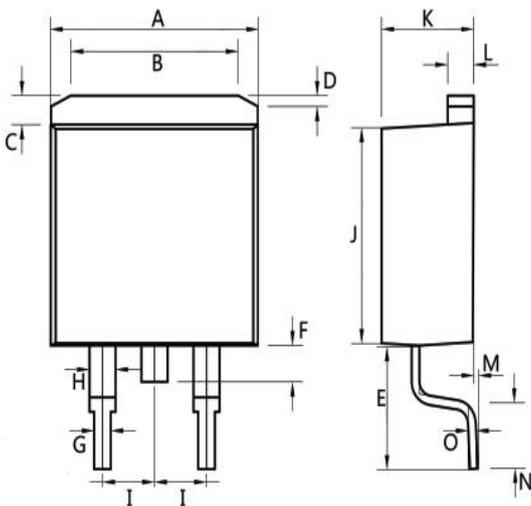
### Package Outline

T0-220 封装尺寸 (Package size)



Dim	Min	Max
A	10	10.4
B	2.5	3
C	3.5	4
D	28	30
E	1.1	1.5
F	6.2	6.6
G	2.9	3.3
H	15	16
I	0.35	0.45
J	4.3	4.7
K	1.2	1.4
L	Typ 5.08	
M	Typ 2.54	
N	3.1	3.5
O	0.7	0.9
P	10	10.4

T0-263 封装尺寸 (Package size)



Dim	Min	Max
A	10	10.5
B	7.25	7.75
C	1.3	1.5
D	0.55	0.75
E	5	6
F	1.4	1.6
G	0.75	0.95
H	1.15	1.35
I	TYP 2.54	
J	8.4	8.6
K	4.4	4.6
L	1.25	1.45
M	0.02	0.1
N	2.4	2.8
O	0.35	0.45