YK080N04-D3

N-Channel Enhancement Mode Field Effect Transistor

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General Description

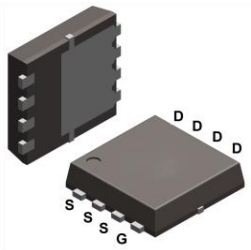
The YK080N04-D3 uses advanced trench technology and design to provide excellent RDS(ON) with low gate charge. It can be used in a wide variety of applications.

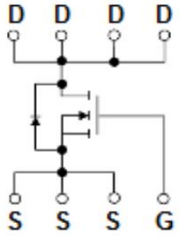
Application

- Load switching
- Hard switched and high frequency circuits
- Uninterruptible power supply

Features

- V_{DS} = 40V,I_D = 40A
  $R_{DS(ON)}$ <8mΩ @V_{GS}=4.5V
  $R_{DS(ON)}$ <10mΩ @V_{GS}=10 V
- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Good stability and uniformity with high EAS
- Excellent package for good heat dissipation
- Special process technology for high ESD capability





Package Marking and Ordering Information

Device Marking	Device	Device Package	Quantity
080N04	YK080N04-D3	PDFN3×3-8L	5000 pcs / Tape & Reel

Absolute Maximum Ratings (T_A=25°Cunless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DSS}	40	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current-Continuous V_{GS}=4.5V，@Ta=25°C	I_D	40	A
Pulsed Drain Current(Note 2)	I_{DM}	120	A
Maximum Power Dissipation @Ta=25°C	P_D	25	W
Single pulse avalanche energy (Note 3)	EAS	78	mJ
Operating Junction and Storage Temperature Range	T_J	-55 ~ +150	°C

Thermal Characteristics

Thermal Resistance Junction-to-Case（Note1）	$R_{\theta JC}$	5	°C/W

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Electrical Characteristics (T_A=25℃ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D= 250μA	40		-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 32V, V_{GS}= 0V	-	-	1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS} = ±20V,V_{DS} = 0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_{DS}= 250μA	1.2	-	2.5	V
Drain-Source On-State Resistance （NOT2)	$R_{DS(ON)}$	V_{GS}= 4.5V, I_{DS}=10A	-	-	10	mΩ
		V_{GS} =10V, I_{DS}= 12A	-	-	8	
Dynamic Characteristics						
Input Capacitance	C_{iss}	VGS = 0V VDS = 15V f = 1.0MHz	-	2330	-	pF
Output Capacitance	C_{oss}		-	195	-	
Reverse Transfer Capacitance	C_{rss}		-	138	-	
Switching Characteristics						
Turn-on Delay Time	$T_{d(on)}$	VDD = 15V VGS = 10V RG = 3.3Ω ID = 1A	-	14.3	-	ns
Turn-on Rise Time	T_r		-	2.6	-	
Turn-Off Delay Time	$T_{d(OFF)}$		-	77	-	
Turn-Off Fall Time	T_f		-	4.8	-	
Total Gate Charge	Q_g	VDD = 20V VGS = 4.5V ID = 20A	-	18.8	-	nC
Gate-Source Charge	Q_{gs}		-	4.7	-	
Gate-Drain Charge	Q_{gd}		-	8.2	-	
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 2)	V_{SD}	I_{SD} = 1A, VGS = 0V, T_J = 25°C	-	-	1.2	V
Diode Forward Current (Note 1、4)	I_S		-	-	70	A

Notes:

1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper

2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%

3. The EAS data shows Max. rating. The test condition is VDD = 25V, VGS = 10V, L = 0.5mH

4. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation

Typical Electrical and Thermal Characteristics

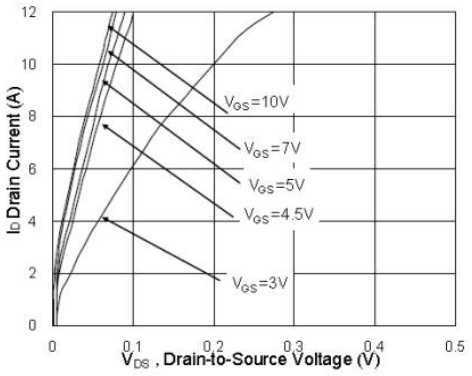


Fig 1 Typical Output Characteristics

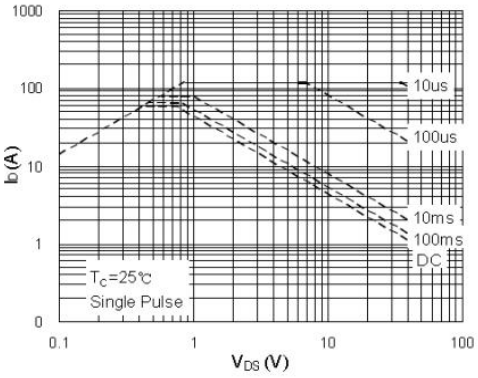


Fig 2 Maximum Safe Operating Area

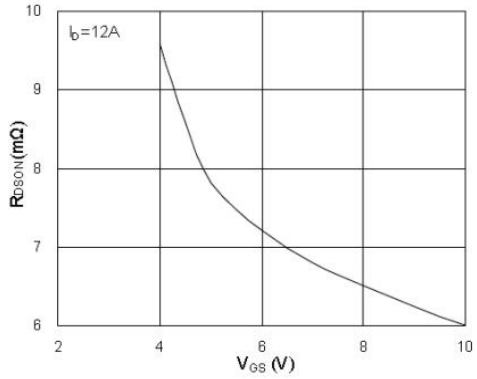


Fig 3 On-Resistance vs. Gate-Source Voltage

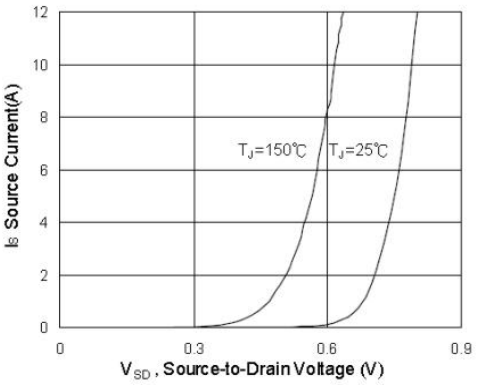


Fig 4 Body-Diode Characteristics

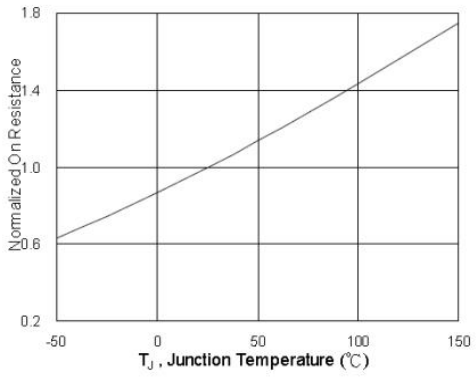


Fig 5 On-Resistance vs. Junction Temperature

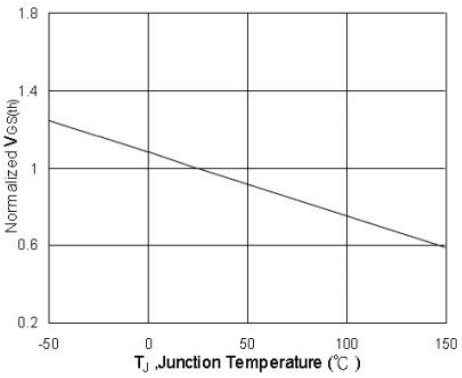


Fig 6 Gate Threshold Voltage vs. Junction Temperature

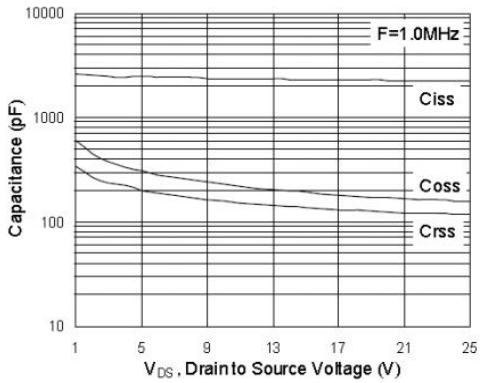


Fig 7 Capacitance Characteristics

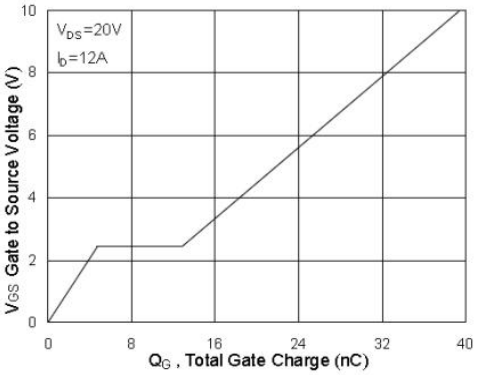
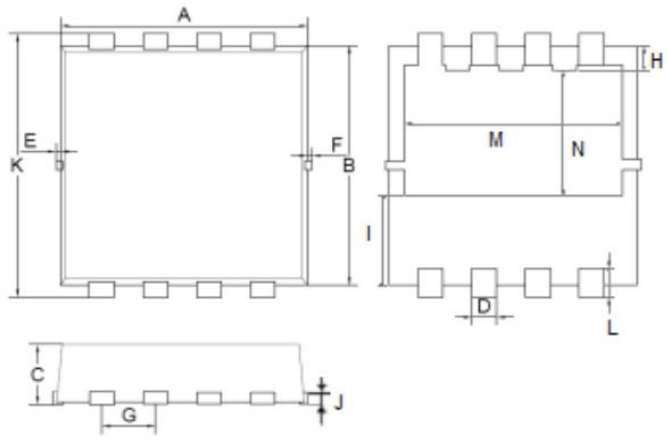


Fig 8 Gate-Charge Characteristics

PDFN3*3-8L Package Information



PDFN3×3-8L		
Dimension	**Min.**	**Max.**
A	2.90	3.10
B	2.90	3.10
C	0.65	0.85
D	0.20	0.40
E	0.00	0.10
F	0.00	0.10
G	0.55	0.75
H	0.20	0.40
I	0.70	1.10
J	0.10	0.20
K	3.15	3.45
L	0.20	0.40
M	2.35	2.55
N	1.500	1.900