YK900P04

P-Channel Enhancement Mode Field Effect Transistor

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General Description

The YK900P04 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a load switch or in PWM applications.

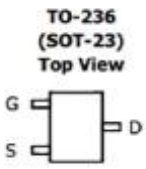
Application

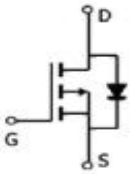
- PWM application
- Load switch
- Power management

Features

V_{DS} = -40V,I_D = -3A
$R_{DS(ON)}$ <85mΩ @V_{GS}=-10V
$R_{DS(ON)}$ <100mΩ @V_{GS}=-4.5V

- High power and current handing capability
- Lead free product is acquired
- Surface mount package





Package Marking and Ordering Information

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
900P04	YK900P04	SOT-23	Ø180mm	8mm	3000 units

Absolute Maximum Ratings (T_A=25°Cunless otherwise noted)

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DSS}	-40	V
Gate-Source Voltage	V_{GSS}	±20	V
Drain Current-Continuous V_{GS}=-4.5V，@Ta=25°C （Note1)	I_D	-3	A
Drain Current –Pulsed	I_{DM}	-30	A
Maximum Power Dissipation @Ta=25°C	P_D	2.5	W
Single pulse avalanche energy (Note 3)	EAS	11	mJ
Operating Junction and Storage Temperature Range	T_J	-55 ~ +150	°C

Thermal Characteristics

Thermal Resistance,Junction-to-Ambient（Note 1)	$R_{\theta JA}$	100	°C/W

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Electrical Characteristics (T_A=25°C unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D= -250μA	-40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -40V, V_{GS}= 0V	-	-	-1	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS} = ±20V,V_{DS} = 0V	-	-	±100	nA
On Characteristics						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_{DS}= -250μA	-1	-1.4	-2.5	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}= -10V, I_{DS}= -3A	-	60	85	mΩ
		V_{GS}= -4.5V, I_{DS}= -2A	-	70	100	
Gate Resistance	Rg	VGS = 0V, f = 1MHz	-	25	-	Ω
Dynamic Characteristics						
Input Capacitance	C_{iss}	VGS = 0V VDS = -20V f = 1.0MHz	-	597	-	pF
Output Capacitance	C_{oss}		-	51	-	
Reverse Transfer Capacitance	C_{rss}		-	41	-	
Switching Characteristics						
Turn-on Delay Time (Note 4)	$T_{d(on)}$	VDD = -20V VGS = -10V ID = -5A RG = 2.5Ω	-	6.5		ns
Turn-on Rise Time (Note 4)	T_r		-	14		
Turn-Off Delay Time (Note 4)	$T_{d(OFF)}$		-	34		
Turn-Off Fall Time (Note 4)	T_f		-	18		
Total Gate Charge	Q_g	VDD = -20V VGS = -10V ID = -3A	-	14.5	-	nC
Gate-Source Charge	Q_{gs}		-	2.4	-	
Gate-Drain Charge	Q_{gd}		-	2.1	-	
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 2)	V_{SD}	I_S =-5A, V_{GS}=0V Tj = 25°C	-	-	-1.2	V

Notes:

1.The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper

2. The data tested by pulsed, pulse width ≤ 300μs, duty cycle ≤ 2%

3.The EAS data shows Max. rating. The test condition is VDD = 25V, VGS = 10V, L = 0.1mH

4. Guaranteed by design, not subject to production

Typical Electrical and Thermal Characteristics

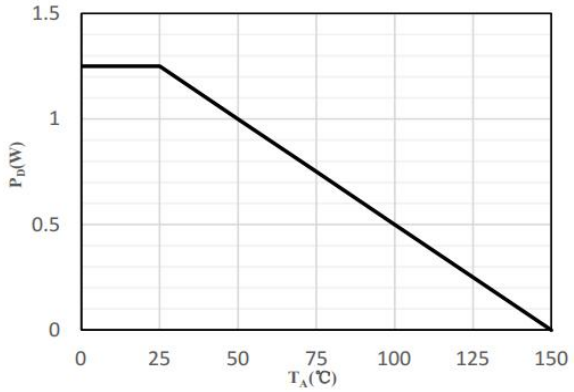


Fig 1 Power Dissipation

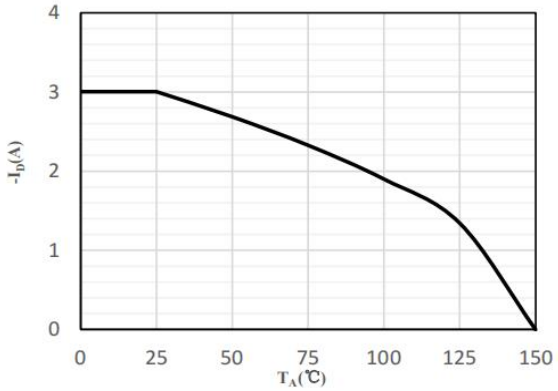


Fig 2 Drain Current

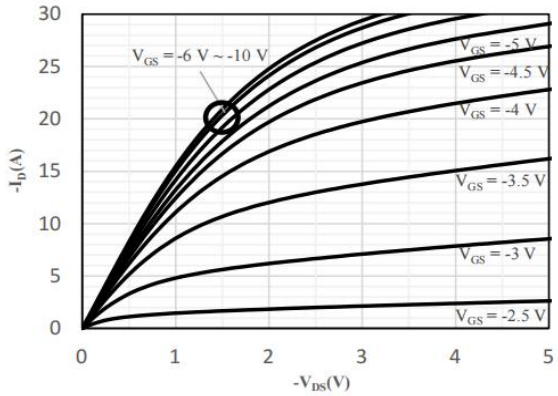


Fig 3 Typical Output Characteristics

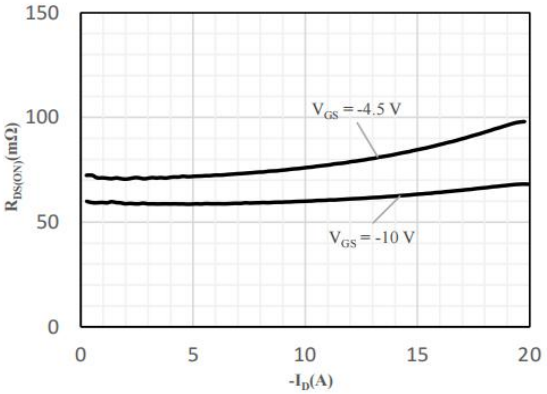


Fig 4 On-Resistance vs. Drain Current and Gate Voltage

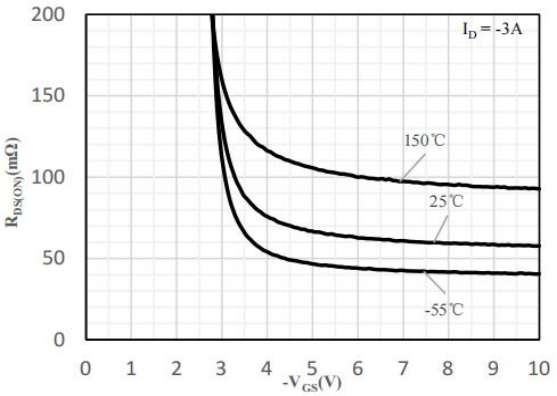


Fig 5 On-Resistance vs. Gate-Source Voltage

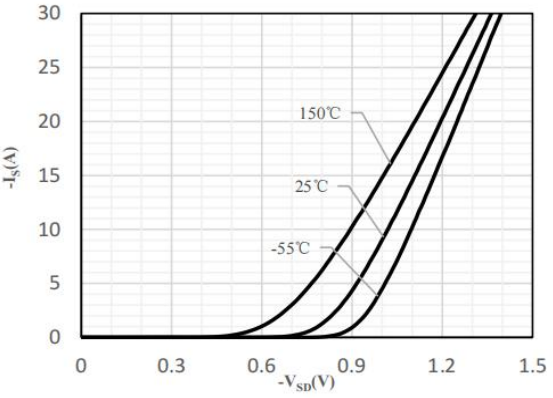


Fig 6 Body-Diode Characteristics

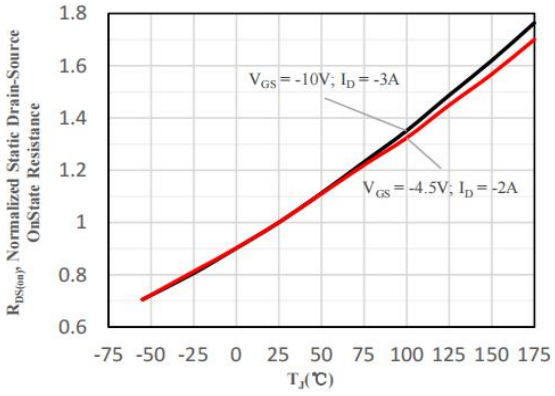


Fig 7 Normalized On-Resistance vs. Junction Temperature

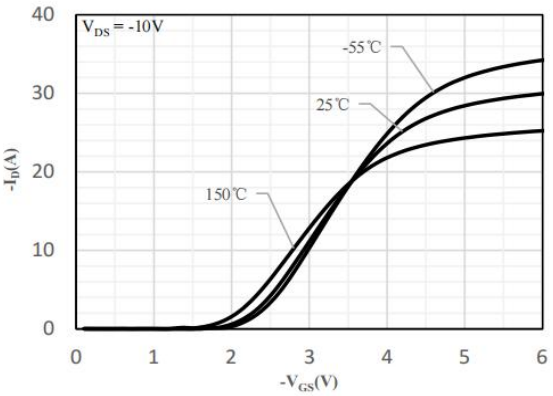


Fig 8 Transfer Characteristics

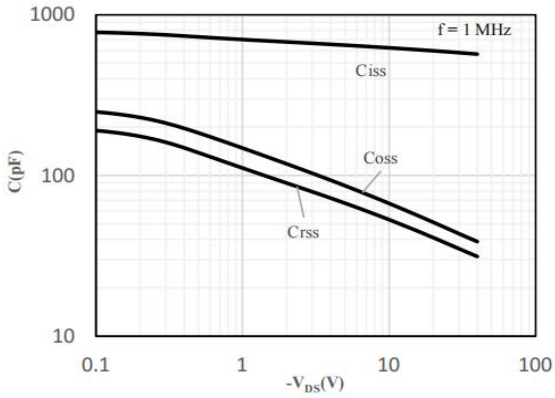


Fig 9 Capacitance Characteristics

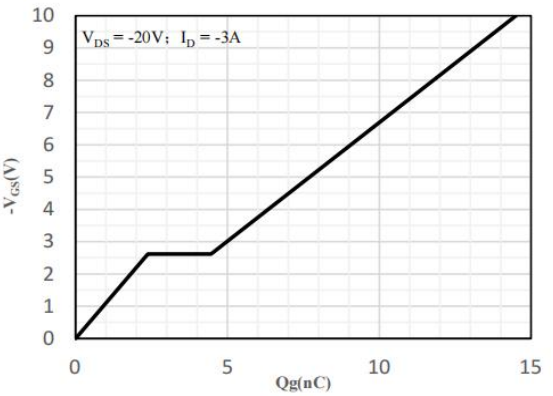


Fig 10 Gate-Charge Characteristics

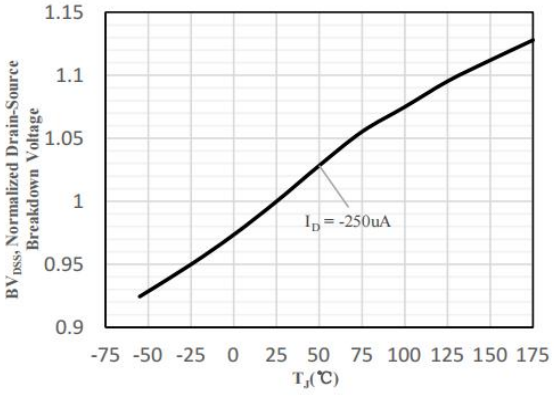


Fig 11 Normalized Breakdown Voltage vs. Junction Temperature

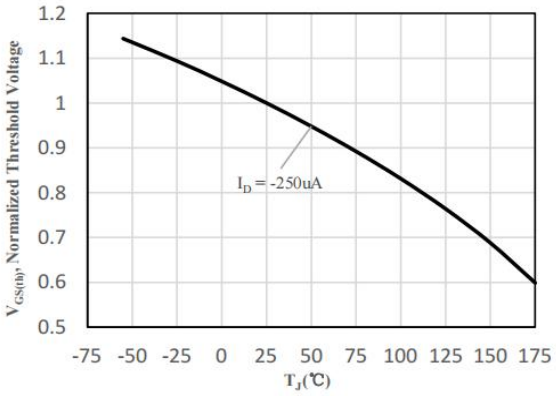


Fig 12 Normalized $V_{GS(th)}$ vs. Junction Temperature

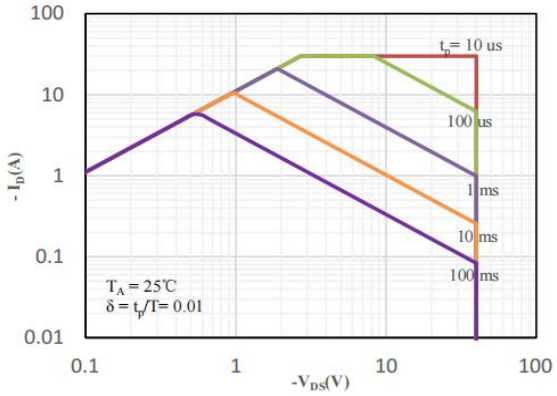


Fig 13 Safe Operation Area

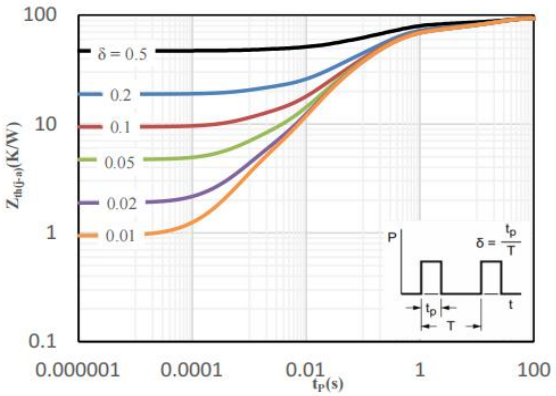
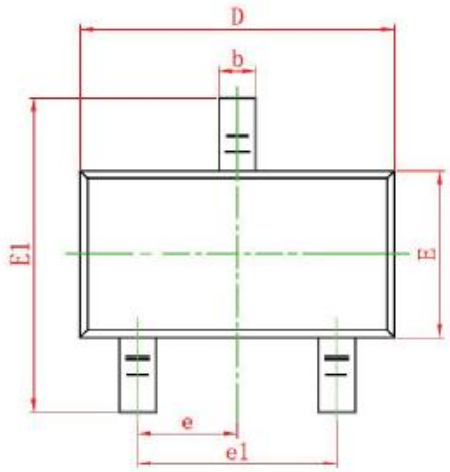
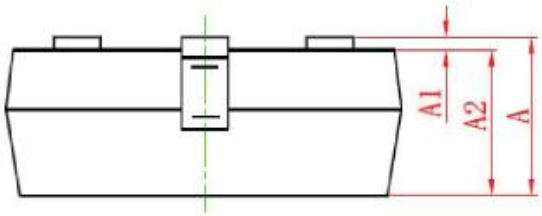
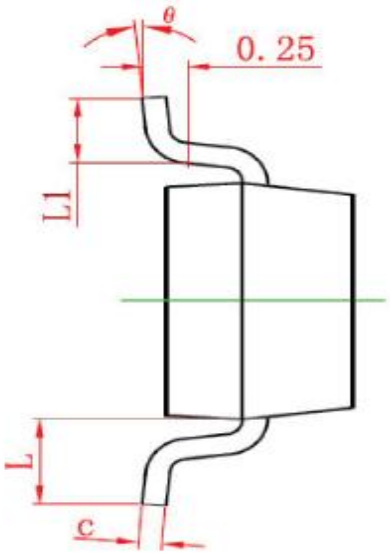


Fig 14 Maximum transient thermal impedance

SOT-23 Package Information







Symbol	Dimensions in Millimeters	
	MIN	MAX
A	0.900	1.150
A1	0.000	0.100
A2	0.900	1.050
b	0.300	0.500
C	0.080	0.150
D	2.800	3.000
E	1.200	1.400
E1	2.250	2.550
e	0.950 TYP	
e1	1.800	2.000
L	0.550 REF	
L1	0.300	0.500
θ	0°	8°